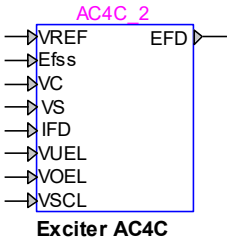
Exciters and Governors: Exciter AC4C



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1 Description

This device is an implementation of the IEEE type AC4C excitation system model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 7 pins:

Pin name	Type	Description	Units
VREF	Input	Reference voltage of the stator terminal voltage	pu
Efss	Input	Steady-state field voltage at t = 0, for initialization	pu
VC	Input	Terminal voltage of synchronous machine, transducer output	pu
VS	Input	Power System Stabilizer signal	pu
IFD	input	Field current	pu
VUEL	Input	Under Excitation Limiter signal	pu
VOEL	Input	Over Excitation Limiter signal	pu
VSCL	Input	Stator Current Limiter signal	pu
EFD	Output	The field voltage signal	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Time constant T_B**: Regulator denominator (lag) time constant
2. **Time constant T_C**: Regulator numerator (lead) time constant
3. Under Excitation Limiter option: see explanations below.

4. Over Excitation Limiter option: see explanations below.
5. Stator Current Limiter option: see explanations below.

There are two possible selections for the Under Excitation Limiter option:

1. VUEL not available or added to the reference voltage: this option can be selected when the VUEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VUEL connected to the high value gate (HV gate)

There are two possible selections for the Over Excitation Limiter option:

1. VOEL not available or added to the reference voltage: this option can be selected when the VOEL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VOEL connected to the low value gate (LV gate).

There are three possible selections for the Stator Current Limiter option:

1. VSCL not available or added to the reference voltage: this option can be selected when the VSCL input signal is zero (not connected) or when it is connected and added to the reference voltage.
2. VSCL connected to the high value gate (HV gate).
3. VSCL connected to the low value gate (LV gate).

1.2.2 Exciter tab

The exciter tab allows to input:

1. **Gain K_A**: Voltage regulator gain
2. **Time constant T_A**: Voltage regulator time constant
3. **Rectifier loading factor K_C**: Rectifier loading factor proportional to commutating reactance
4. **Maximum regulator input V_{IMAX}**: Voltage regulator input (voltage error) maximum limit
5. **Minimum regulator input V_{IMIN}**: Voltage regulator input (voltage error) minimum limit
6. **Maximum regulator output V_{RMAX}**: Maximum regulator voltage output
7. **Minimum regulator output V_{RMIN}**: Minimum regulator voltage output

2 Initial conditions

The reference voltage VREF can be manually or automatically set by connecting or not connecting the input signal VREF, respectively. When VREF is not connected (the signal is zero), the reference voltage is internally found from the steady-state solution. When VREF is connected, its initial value must match the per unit steady-state voltage of the stator terminal voltage, since otherwise the generator voltage will not start at the actual steady-state.

3 References

[1] “IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies,” IEEE Standard 421.5-2016.