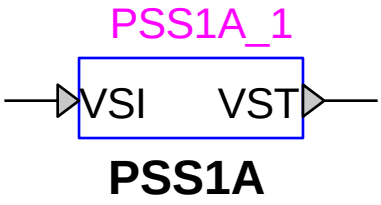
Exciters and Governors: Power System Stabilizer PSS1A



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1 Description

This device is an implementation of the IEEE type PSS1A power system stabilizer model. This device is implemented as described in [1]. Implementation details can be viewed by inspecting the subcircuit of this device.

1.1 Pins

This device has 2 pins:

Pin name	Type	Description	Units
VSI	Input	Synchronous machine speed deviation or acceleration power	pu
VST	Output	PSS output (equivalent of terminal voltage)	pu

1.2 Parameters

The default set of parameters can be found in [1].

1.2.1 Data tab

The parameters on the Data tab are:

1. **Time constant T_5**: transducer time constant
2. **Time constant T_6**: transducer time constant
3. **Gain K_S**: power system stabilizer gain
4. **Filter constant A_1**: PSS signal conditioning frequency filter constant
5. **Filter constant A_2**: PSS signal conditioning frequency filter constant
6. **Lead time constant T_1**: Lead time constant
7. **Lead time constant T_3**: Lead time constant
8. **Lag time constant T_2**: Lag time constant

9. **Lag time constant T_4**: Lag time constant
10. **Maximum output V_{STMAX}**: PSS maximum output signal
11. **Minimum output V_{STMIN}**: PSS minimum output signal

2 Initial conditions

The initial output signal is zero from the steady-state solution.

3 References

[1] "IEEE Recommended Practice for Excitation System Models for Power System Models for Power System Stability Studies," IEEE Standard 421.5-2005.